Claims

[1] 1. A laminated chip element, comprising:
at least one first sheet on which first and second conductive patterns are formed, the first and second conductive patterns being spaced apart from each other in a direction of both ends of the first sheet; and
at least one second sheet on which a third conductive pattern is formed, the third conductive pattern being formed in a transverse direction of both the ends of the first sheet;
wherein one ends of the first and second conductive patterns are connected to first and second external terminals, respectively, at least one end of the third conductive pattern is connected to a third external terminal, and the first and second sheets are laminated.

[2] 2. A laminated chip element according to claim 1, wherein the first and second sheets are alternately laminated on each other.

[3] 3. A laminated chip element, comprising:
at least one first sheet on which first and second conductive patterns are formed, the first and second conductive patterns being spaced apart from each other in a direction of both ends of the first sheet; and
at least one second sheet on which a third conductive pattern is formed, the third conductive pattern consisting of first and second portions which are spaced apart from each other and formed in a transverse direction of both the ends of the first sheet;
wherein one ends of the first and second conductive patterns are connected to first and second external terminals, respectively, both opposite ends of the first and second portions of the third conductive pattern are connected to third and fourth external terminals, respectively, and the first and second sheets are laminated.

[4] 4. A laminated chip element according to claim 3, wherein the first and second sheets are alternately laminated on each other.

[5] 5. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed in a direction of both ends of the first sheet; and
at least one second sheet on which a second conductive pattern is formed in the same direction of the first conductive pattern,

at least one third sheet on which a third conductive pattern is formed in a transverse direction of both the ends of the first sheet;
wherein one ends of the first and second conductive patterns are connected to first and second external terminals, respectively, at least one end of the third conductive pattern is connected to a third external terminal, and the first to third sheets are laminated.

[6] 6. A laminated chip element according to claim 5, wherein the first to third sheets are laminated so that one or more of the third sheets are interposed between the first sheet and the second sheet.

[7] 7. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed in a direction of both ends of the first sheet;
at least one second sheet on which a second conductive pattern is formed in the same direction of the first conductive pattern;
at least one third sheet on which a third conductive pattern is formed in a transverse direction both the ends of the first sheet; and
at least one fourth sheet on which a fourth conductive pattern is formed in the same direction of the third conductive pattern;
wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, respectively, both opposite ends of the third and fourth conductive patterns are connected to third and fourth external terminals, respectively, and the first to fourth sheets are laminated.

[8] 8. A laminated chip element according to claim 7, wherein the third and fourth sheets are interposed between the first sheet and the second sheet.

[9] 9. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed in a direction of both ends of the first sheet;
at least one second sheet on which a second conductive pattern is formed in the same direction of the first conductive pattern; and
at least one third sheet on which a third conductive pattern is formed in the same direction of the first conductive pattern;
wherein both opposite ends of the first and second conductive patterns are connected to first and second external terminals, respectively, an end of the third conductive pattern is connected to a third external terminal, and the first to third sheets are laminated.

[10] 10. A laminated chip element according to claim 9, wherein a first laminate consisting of two of the first sheets and one of the third sheets interposed between the two first sheets and a second laminate consisting of two of the second sheets and one of the third sheets interposed between the two second sheets, are laminated on each other.

[11] 11. A laminated chip element according to claim 9, wherein one or more of the third sheets are interposed between the first sheet and the second sheet.

[12] 12. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed, the first conductive pattern consisting of first to third portions, the first and second portions being spaced apart from each other in a direction of both ends of the first sheet, the third portion being spaced apart from the first and second portions and formed in a transverse direction of both the ends of the first sheet; and
at least one second sheet on which a second conductive pattern is formed, the second conductive pattern consisting of fourth and fifth portions, the fourth portion partially overlapping with the first and third portions, the fifth portion partially overlapping with the second and third portions;
wherein one ends of the first and second portions are connected to first and second external terminals, respectively, at least one end of the third portion is connected to a third external terminal, and the first and second sheets are laminated.

[13] 13. A laminated chip element according to claim 12, wherein the first and second sheets are alternately laminated on each other.

[14] 14. A laminated chip element according to any one of claims 1 to 13, wherein areas of overlapping portions between the conductive patterns differ from each other.

[15] 15. A laminated chip element, wherein a plurality of the laminated chip elements according to any one of claims 1 to 13 are arranged in parallel with each other and integrally manufactured in an array.

[16] 16. A laminated chip element according to any one of claims 1 to 13, wherein a resistive pattern is formed on the laminated chip element , and both ends of the resistive pattern are connected to the first and second external terminals, respectively.

[17] 17. A laminated chip element according to claim 16, wherein two metal pads are formed in spaced relation with each other, and the resistive pattern is formed so

that the resistive pattern connects the two metal pads to each other.

[18] 18. A laminated chip element according to any one of claims 1 to 13, further comprising at least one resistor sheet on each of which a resistive pattern is formed, wherein said at least one resistor sheet is further laminated.

[19] 19. A laminated chip element according to claim 16, wherein an insulated pattern or layer is formed on the uppermost one of the laminated sheets.

[20] 20. A laminated chip element according to claim 16, wherein a resistive pattern comprises resistive material, such as Ni-Cr or RuO_2.

[21] 21. A laminated chip element, wherein a plurality of the laminated chip elements according to claim 16 are arranged in parallel with each other and integrally manufactured in an array.

[22] 22. A laminated chip element according to any one of claims 1 to 13, wherein an inductive pattern is formed on the laminated chip element , and both ends of the inductive pattern are connected to the first and second external terminals, respectively.

[23] 23. A laminated chip element according to claim 22, wherein two metal pads are formed in spaced relation with each other, and the inductive pattern is formed so that the inductive pattern connects the two metal pads to each other.

[24] 24. A laminated chip element according to claim 22, wherein an insulated pattern or layer is formed on the uppermost one of the laminated sheets.

[25] 25. A laminated chip element, wherein a plurality of the laminated chip elements according to claim 22 are arranged in parallel with each other and integrally manufactured in an array.

[26] 26. A laminated chip element, wherein a plurality of the laminated chip elements according to any one of claims 1 to 13 are arranged in parallel with each other and integrally manufactured in an array, inductive patterns for some of said plurality of the laminated chip elements are formed on an upper surface of the laminated chip element , inductive patterns for the others of said plurality of the laminated chip elements are formed on a lower surface of the laminated chip element , and both ends of the respective inductive patterns are connected to the corresponding first and second external terminals.

[27] 27. A laminated chip element according to claim 22, wherein the inductive pattern is spiral, an insulated bridge is formed in a radial direction across the spiral inductive pattern, and a bridge pattern for extending a center end of the inductive pattern to an outside thereof is formed on the insulated bridge.

[28] 28. A laminated chip element according to claim 22, wherein a ferrite layer is form on the laminated chip element, and the inductive pattern is formed on the ferrite layer.

[29] 29. A laminated chip element according to claim 22, wherein the inductive pattern comprises metal material , such as Ag, Pt, Pd.

[30] 30. A laminated chip element according to claim 22, wherein the inductive pattern comprises resistive material, such as Ni-Cr, RuO_2.

[31] 31. A laminated chip element, wherein a plurality of the laminated chip elements according to any one of claims 1 to 13 are arranged in parallel with each other and integrally manufactured in an array, a plurality of inductor sheet s are further laminated, at least one inductive pattern is formed on each of the inductor sheet s, and both ends of the respective inductive patterns are connected to the corresponding first and second external terminals.

[32] 32. A laminated chip element according to claim 31, wherein the inductive pattern is meander-shaped.

[33] 33. A laminated chip element according to any one of claims 1 to 13, wherein a plurality of inductor sheet s are further laminated, an inductive pattern is formed on each of the inductor sheets, the inductive patterns are connected to each other in series through through holes formed in the inductor sheets, both ends of the connected inductive patterns are connected to the first and second external terminals, respectively.

[34] 34. A laminated chip element according to claim 33, wherein the inductor sheets comprises

a first inductor sheet on which a first inductive pattern is formed, one end of the first inductive pattern being extended to an edge of the first inductor sheet, a through hole being formed at the other end of the first inductive pattern;

a second inductor sheet on which a second inductive pattern is formed, one end of the second inductive pattern being extended to an edge of the second inductor sheet, a through hole being formed at the other end of the second inductive pattern; and

at least one third inductor sheet on which a third inductive pattern is formed, a through hole being formed at each of both ends of the third inductive pattern;

wherein the third inductor sheet is interposed between the first and second inductor sheets, the through holes are filled with conductive material, said one ends of the first and second inductive patterns are connected to the first and

second external terminals, respectively, and the first to third inductive patterns are connected to each other through the conductive material filled in the through holes.

[35] 35. A laminated chip element according to claim 33, wherein the inductive patterns are formed in the direction of the first and second external terminals.

[36] 36. A laminated chip element according to claim 33, wherein the through holes are filled with conductive material in order to connect the inductive patterns to each other.

[37] 37. A laminated chip element, wherein a plurality of the laminated chip elements according to claim 33 are arranged in parallel with each other and integrally manufactured in an array.

[38] 38. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed, the first conductive pattern consisting of first to third portions, the first and second portions being spaced apart from each other in a direction of both ends of the first sheet, the second portion connecting the first and second portions to each other to have a predetermined inductance; and
at least one second sheet on which a second conductive pattern is formed in a transverse direction of both the ends of the first sheet;
wherein the first and second portions are connected to first and second external terminals, respectively, at least one ends of the second conductive pattern is connected to a third external terminal, and the first and second sheets are laminated.

[39] 39. A laminated chip element according to claim 38, wherein a plurality of the first sheets and the second sheets are alternately laminated on each other, and the first and second portions of the first conductive patterns formed on the respective first sheets are connected to the respective first and second external terminals.

[40] 40. A laminated chip element, comprising:
at least one first sheet on which a first conductive pattern is formed in a direction of both ends of the first sheet; and
at least one second sheet on which a second conductive pattern is formed in the same direction of the first conductive pattern;
wherein both ends of the first conductive pattern are connected to first and second external terminals, respectively, a terminal connecting portion of the second conductive pattern is connected to a third external terminal, and the first

and second sheets are laminated.

[41] 41. A laminated chip element according to claim 40, wherein the terminal connecting portion is an end of the second conductive pattern.

[42] 42. A laminated chip element according to claim 40, wherein the terminal connecting portion is an intermediate portion of the second conductive pattern.

[43] 43. A laminated chip element according to claim 40, wherein the terminal connecting portion is both opposite ends of the second conductive pattern.

[44] 44. A laminated chip element according to any one of claims 40 to 43 , wherein a plurality of the first and second conductive patterns are formed in parallel with each other on the corresponding sheets so that a plurality of unit elements are integrally manufactured into the laminated chip element , the terminal connecting portions of two outermost ones of the second conductive patterns are connected to the third external terminal, the terminal connecting portions of the other second conductive patterns are connected to the terminal connecting portions of the adjacent second conductive patterns one to one, and both ends of each of the first conductive patterns are connected to the first and second external terminals for each unit element.

[45] 45. A laminated chip element according to any one of claims 40 to 43, wherein one or more of the second sheets are interposed between two of the first sheets.

[46] 46. A laminated chip element according to any one of claims 38 to 43 , wherein the sheets comprise ferrite sheets.

[47] 47. A laminated chip element according to any one of claims 1 to 13 and 38 to 43 , wherein the sheets comprise ceramic sheets.

[48] 48. A laminated chip element according to any one of claims 1 to 13 and 38 to 43 , wherein the sheets comprise varistor sheets.

[49] 49. A laminated chip element according to any one of claims 1 to 13 and 38 to 43 , wherein the sheets comprise PTC thermistor sheets.

[50] 50. A laminated chip element according to any one of claims 1 to 13 and 38 to 43 , wherein the sheets comprise NTC thermistor sheets.

[51] 51. A laminated chip element according to any one of claims 1 to 13 and 38 to 43 , wherein the conductive patterns comprise metal material, such as Ag, Pt, Pd.

[52] 52. A laminated chip element according to any one of claims 38 to 43 , wherein the second conductive pattern comprises resistive material, such as Ni-Cr, RuO_2.